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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/798,213 | 03/10/2004 | Tino Hellberg | 874.0109.U2(US) | 6131 |

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| EXAMINER | |
|---|---|
| DANG, KHANH | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2111 | |

DATE MAILED: 05/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/798,213 | HELLBERG, TINO | |
| | Examiner | Art Unit | |
| | Khanh Dang | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *3/10/2004 AMENDMENT*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3 and 8-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,8 and 39-41* is/are allowed.

6)☒ Claim(s) *9-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/10/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Applicants' preliminary Amendments filed 3/10/2004 with this continuation application is acknowledged.

### Basis for Nonstatutory Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 9-38 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3, and 8-33 of U.S. Patent No. 6,742,061. Although the conflicting claims are not identical, they are not patentably distinct from each other because there are only minor changes to the claims. For example, the terms: "interface circuit" and "a bit serial bidirectional signal line" in claim 8 of U.S. Patent No. 6,742,061 have been replaced by the terms "interface" and "a serial bidirectional line," respectively, in claim 9 of the instant application.

Further, since these claims, if allowed, would improperly extend the "right to exclude" already granted in the patent. The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: for example, claim 8 of U.S. Patent No. 6,742,061 is directed to an interface circuit for coupling a slave device to a master device, said interface supporting a bit serial data bidirectional signal line that conveys commands and associated data from said master device to said slave device, said bit serial data bidirectional signal line further conveying other signals, said other signals comprising a reset signal, an interrupt signal, and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device, where said interface comprises, in said slave device, an Accessory Control Interface chip with an oscillator providing a clock signal to said Accessory Control Interface chip, where the bit time is a multiple of the clock signal, and

where said master device adapts by sampling of the data transferred from said slave device in accordance with the specified duration of the bit time.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See In re Schneller, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP Section 804.

**Allowable Subject Matter**

Claims 1-3, 8, and 39-41 are allowed.

**Reasons for Allowance**

The prior art of record does not disclose the following limitations to be used in combination with "the interface" set forth in claim 1, the "master device" set forth in claims 39 and 41, and the "slave device" set forth in claim 39:

"said interface comprises a resistance R coupled between the serial data bidirectional signal line and a circuit ground, and a pull up resistance R.sub.PU installed in the master device, wherein R and R.sub.PU together form a resistor voltage divider network" (claim 1);

"said interface comprises a resistance R coupled between the serial data bidirectional signal line and a ground, and a pull up resistance R.sub.PU installed in the

master device, wherein R and R.sub.PU together form a resistor voltage divider network" (claim 39).

"said interface comprises a resistance R coupled between the serial data bidirectional signal line and a ground, and a pull up resistance R.sub.PU installed in the master device, wherein R and R.sub.PU together form a resistor voltage divider network" (claim 40).

"the interface comprises a resistance R coupled between the serial data bidirectional signal line and a ground, and a pull up resistance R.sub.PU installed in the master device, wherein R and R.sub.PU together form a resistor voltage divider network, wherein presence of the resistance R affects the serial data bidirectional signal line to enable detection of a slave device connected/disconnected state."

US Patent No. 5,210,846 to Lee, 5,708,799 to Gafken et al., and 6,532,506 to Dunstan et al. are cited as relevant art.

Maxim, Overview of 1-Wire Technology and Its Use, Maxim, Creating Non-Linear Tranfer Functions With Linear Potentiomater Circuits, Definition of 1-Wire Bus by Wikipedia, and Definition of Voltage Divider Rule from Wikipedia are also cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 571-272-3626.

Khanh Dang
Primary Examiner